Advanced High-Performance 320x240 VO_X Microbolometer Uncooled IR Focal Plane

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ABSTRACT

This paper describes Boeing's next-generation 320x240 uncooled IR focal plane product (U4000). The basic objectives have been to at least double focal plane performance, improve focal plane operating stability, and significantly enhance the control interface between the focal plane and the camera. All of these basic objectives have been achieved. Focal plane temporal NETD = 0.028°C (F/1) has been demonstrated at a frame rate of 60 Hz on the first lot of UFPAs produced, as well as a worst-case spatial NETD < 0.016°C (F/1) measured over a 10°C temperature calibration range. Operating stability improvement has been successfully demonstrated. The design has validated a "Smart-Sensor" UFPA/camera control interface that provides externally programmability of on-chip signal gain, on-chip pixel offset compensation, on-chip detector bias regulation, precision on-chip temperature measurement, and a 16 test-point Built In Test (BIT) function. Based on Lot-1 test results, the next lot, which is now in wafer processing, is expected to achieve NETD < 0.02°C (F/1) at a 60 Hz frame rate. With an improved microbolometer Thermal Isolation Structure, currently in development at Boeing, NETD < 0.010°C can be demonstrated before the end of this year.

INTRODUCTION

Under the sponsorship of DARPA and CECOM on the "Infrared Detector Materials Research" BAA program, Boeing has conducted the design, development and demonstration of its next-generation uncooled VO_X microbolometer IR focal plane product, the U4000. The Readout Integrated Circuit design was performed at Indigo Systems Corporation (ISC). The basic objectives for the next-generation design have been to at least double focal plane performance, improve focal plane operating stability, and significantly enhance the capabilities of the control interface between the focal plane and the camera. Table-1 summarizes the basic design approach. Doubled focal plane performance now allows the use of slower, smaller, lower cost optics, while providing enhanced sensitivity with faster optics. A 6-bit on-chip pixel offset compensation function has been incorporated in the design to allow higher levels of on-chip signal gain, while further enhancing the UFPA's response linear dynamic range. Higher signal gain makes the UFPA/camera signal interface easier to implement, and an improved response linear dynamic range significantly enhances the scene temperature range over which effective response and offset compensation can be achieved. Externally programmable on-chip signal gain has been incorporated to provide the capability to achieve a more nearly constant output voltage range for the anticipated range of optics and frame rates. An on-chip detector bias regulator has been incorporated in the design because Boeing's modeling analysis had shown that the level of spatial offset patterning from a microbolometer focal plane is very sensitive to any detector bias drift after calibration. The objective was to provide, on-chip, bias drift rejection of at least 100:1, so that the combination of a 1% external supply and the on-chip bias regulator would achieve bias stability of better than one part in 10^4. An on-chip temperature sensing capability was incorporated to provide a temperature measurement resolution of < 10 mK over an operating temperature range from −20°C to + 60°C. A "Smart-Sensor" data bus interface was incorporated in the design to provide the focal plane with the pixel offset compensation data stored in the camera, and to provide the focal plane with operating mode command words from the camera (e.g. signal gain, detector bias voltage).

Boeing developed and provided the design's functional and performance requirements, fabricated and packaged the UFPAs, and performed all design validation and performance characterization testing. ISC designed the Read-Out Integrated Circuit (ROIC), which was processed at a commercial CMOS foundry.

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U4000 UNCOOLED FOCAL PLANE DESIGN OBJECTIVES/APPROACH	
DESIGN OBJECTIVE	**DESIGN APPROACH(ES)**
Double Performance: • $NETD_{TEMPORAL}$ (F/1) < 0.03°C • $NETD_{SPATIAL}$ (F/1) < 0.01°C • Non-Linearity < ± 0.1%	• **ISC Innovations on Boeing's Microbolometer Bridge Input Circuit** to Achieve Higher Response, Lower Noise, and Higher Operability • **On-Chip Pixel Offset Compensation**, Integrated Directly into Bridge Input Circuit, Allows Higher Response, and Improves Uniformity • Careful **Design Attention to Analog Linearity**, Supported by Detailed End-to-End Design Simulations
Improve Stability:	• **On-Chip Detector Bias Regulator** for Improved Stability and $NETD_{SPATIAL}$ • **Microbolometer Bridge Input Circuit, Pixel Offset Compensation, and Non-Linearity < ± 0.1%** Contribute to Improved Stability Against Operating Temperature Drift
Enhance FPA/Camera Interface:	• **"Smart-Sensor" 6-bit Data Bus** Gives Camera Direct Control of Focal Plane Operation • **Externally Programmable On-Chip Gain** Supports Optics from F/1 to F/2, and both 60 and 30 Hz Frame Rates • **VET** Provides Camera with FPA Built-In-Test

Table 1: Key Elements of the Design Objectives and Approaches for the U4000 Uncooled Focal Plane

U4000 PRODUCT DESCRIPTION

The U4000 has been designed to ensure that its form fit and function are as close to Boeing's U3000 UFPA product family as possible. The pixel center-to-center spacing is 51 μm. The same UFPA vacuum package is used, and the same three external clocks (CLOCK, LSYNC, and FSYNC) provide timing control. Although the minimum horizontal blanking requirement has changed, the U4000's video output can be set by the external clocks to be fully compatible with both the U.S. and PAL TV sync standards. With the addition of the externally programmable on-chip detector bias regulator, the required number of external biases has been reduced from four to three. Table-2 provides a summary of the key design features that have been incorporated into the design of the U4000.

The first key interface change has been the introduction of the 6-bit "Smart-Sensor" data bus, which provides the operating mode control words, and the pixel offset compensation data that are provided by the camera to the UFPA. The second key interface change has been the incorporation of analog measurements of the focal plane's operating temperature, and analog measurements of the UFPA's row reference levels, which appear in the UFPA's video output during horizontal blanking. Other new interface features include the global offset function (VOS), and the Vector Enabled Test function (VET). The VOS function allows the camera to provide the UFPA with analog compensation for the potentially large response offsets that occur whenever the scene ambient temperature differs significantly from the UFPA's operating temperature. The VET function allows the camera to command the UFPA to present any one of 16 on-chip logic test points on its VET output pad.

Figure-1 represents one line time of focal plane video output, both before and after pixel offset compensation. For the purpose of illustration, the on-chip gain has been set to its lowest value, so that the offset patterning before pixel offset calibration is completely contained within the focal plane's non-saturated output voltage range. After pixel offset calibration (Figure-1B), the residual level of offset patterning has been reduced by the equivalent of 6 bits (63:1). Even at the maximum gain setting, the residual peak-to-peak offset patterning level will remain below ~ 25% of the focal plane's output voltage range. As a result of on-chip pixel offset compensation, essentially the entire output dynamic range is available to IR response information, and the focal plane's response uniformity is significantly improved. The pixel offset calibration procedure is relatively simple to perform, and it only needs to be performed once for any selection of detector bias, integration time and operating temperature. After the one-time calibration has been performed, the pixel offset correction coefficients can be stored in non-volatile camera memory for later use, and the compensation is insensitive to the camera's choice of on-chip signal gain.

U4000 DESIGN FEATURES	
Design Feature	**Function**
"Smart-Sensor" Data Bus	6-Bit Data Bus Controls Focal Plane Operation, and Provides Pixel Offset Compensation Data from Camera to UFPA
On-Chip Pixel Offset Compensation	• Adjusts Bias for Each Pixel, Providing 63:1 Reduction in the Size of Pixel Offset Patterning, and Ensuring Offset Patterning < 0.25V at Highest Gain • "Range" Control Enhances Pixel Offset Compensation Sensitivity Through External Selection of any One of Three Offset Sensitivity Levels
On-Chip Detector Bias Regulator	Externally Programmable On-Chip Bias Regulator that Provides Better than 100:1 Bias Drift Rejection from External 5.5V Supply
On-Chip Signal Gain	Externally Programmable On-Chip Gain Range of > 6:1
Reference Select	• Externally Programmable Selection of any Combination of Four References for Each Array Row • Enhances Row Operability Yield, and Reduces Noise
Vector Enabled Test (VET)	Externally Programmable Selection of any of 16 On-Chip Logic Test Points
On-Chip Temperature Camera (TEMP)	• Provides Precision On-Chip Temperature Measurements for Camera • Streamed onto Video Output Line During Horizontal Blanking
Global Video Offset (VOS)	• Externally Controlled Global Analog Video Offset • Can be Used as an Effective Input Referred ALC
CLOCK, LSYNC, FSYNC	Three External Clocks Control Data Rate, Line Rate and Frame Rate
Integration Time	• Externally Programmable Selection of Signal Integration Time by Changing Width of LSYNC clock • Can be Used to Further Extend Focal Plane's Effective Dynamic Range

Table 2: Key Design Features of the U4000 Focal Plane

Figure-1 can also be used to describe the U4000's basic line timing. The minimum line time is divided into 390 pixel periods, with each pixel period equal to one-half cycle of CLOCK. The first ten pixel periods are used by the "Smart-Sensor" bus to input setup control words to the focal plane. During this time interval a null differential-signal reference voltage (VOUTREF) appears on the video output line. Active video appears on the output during the next 320 pixel periods, while at the same time pixel offset coefficients are being downloaded sequentially to the focal plane on the "Smart-Sensor" bus. The REF and TEMP signals appear on the video output line during the last 60 pixel periods of the minimum line time, and VOUTREF appears during the remainder of horizontal blanking. The REF signal is used during the pixel offset calibration procedure to set up the references for each row, and the TEMP signal is used to provide precision measurements of the focal plane's operating temperature. Horizontal blanking can be increased from the minimum by reducing the frequency of the LSYNC clock.

The minimum frame consists of 242 lines. Setup conditions and the pixel offset compensation coefficients are downloaded for the first row of the FPA during the first line time. During the second line time, the first row of the FPA is placed in the sense mode, and the setup conditions and pixel offset compensation coefficients for the second row are downloaded to the FPA. The sampled IR response signals for the first row appear in the output during the third line time. This row-by-row process continues for a minimum of 242 line times, until the 240^{th} detector row of the FPA has been read out. Vertical blanking can be increased from the minimum by reducing the frequency of the FSYNC clock. VOUTREF appears in the output whenever active video, REF, or TEMP is not present.

The TEMP function provides a precision measurement of the focal plane's temperature over a greater than 80°C operating temperature range. This was a challenging requirement because a measurement precision of better than ± 0.01°C was needed.

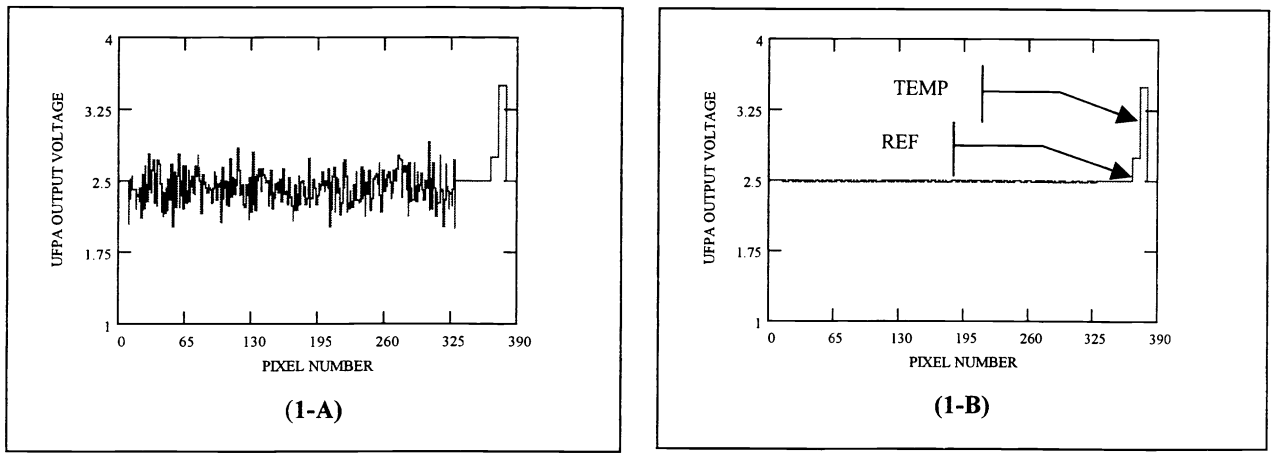

Figure 1: One Line-Time of Active Video Output Both Before (1-A) and After Pixel Offset Compensation (1-B). TEMP and REF Signals are Shown as They Occur During Horizontal Blanking

Six separate TEMP channels are used in the U4000 design to ensure coverage of the operating temperature range with a precision of ± 0.01°C. Further, a temperature coefficient (dV/dT) scale factor of two is used between successive TEMP channels. The output from each TEMP channel appears for eight pixel periods during horizontal blanking, so that sample averaging can be used to improve TEMP signal-to-noise relative to the electronic noise of the focal plane. Further, 32 separate measurements are performed for each TEMP channel during each frame time, and the measurements appear in the video output during 32 consecutive line times. In this way, averaging can also be used to reduce the impact of the voltage bias noise on each of the of the TEMP channels. In operation, the IR camera selects one of the outputs that is close to the TEMP response mid-range to measure the focal plane's operating temperature.

Figure-2 shows the results of a detailed Monte Carlo simulation modeling of the focal plane's expected F/1 spatial NETD for operation at 295K, at frame rate of 60 Hz. The model incorporates the non-uniformities of the VO_X microbolometers and the microbolometer thermal isolation structures, as well as the non-linearity introduced by the microbolometers and the focal plane electronics. The statistical parameter values used in the simulation model were based on measured variations in microbolometer resistance (~ 2% peak-to-peak) and in focal plane response (~ 4% σ/μ). The spatial NETD estimates, which are plotted as functions of IR black-body scene temperature, were determined from the RMS values of residual spatial patterning obtained in the simulation after performing a 2-point response and offset calibration. The model was also used to provide an assessment of the effects of shift in optics temperature, FPA operating temperature and detector bias from the values that were present at the time of calibration. The impact of temporal noise, which is introduced during both calibration and spatial NETD measurement, is also shown. The model indicates that the expected level of spatial pattern noise, due to non-uniformity and non-linearity, is very low for the U4000 focal plane. The level of sensitivity to detector bias drift, however, is very large. On the basis of a predicted $\partial NETD/\partial V \sim 17°C/Volt$ (F/1), the required bias stability for a spatial NETD stability of ~ 0.01°C would have to be < 200 parts/million. This is the reason the U4000 design incorporates an on-chip bias regulator. The on-chip regulator, interfaced to a 1% external supply, is designed to achieve a detector bias stability of better than 100 parts/million. Thus, an external bias supply with a $V^{-1}\partial V/\partial T \sim 10^{-4}/K$ can now be used effectively over a 100°C ambient range. The relative impact of residual temporal noise is also significant. This is a result of the VO_X microbolometer 1/f noise, whose relative magnitude can not be reduced by sample averaging.

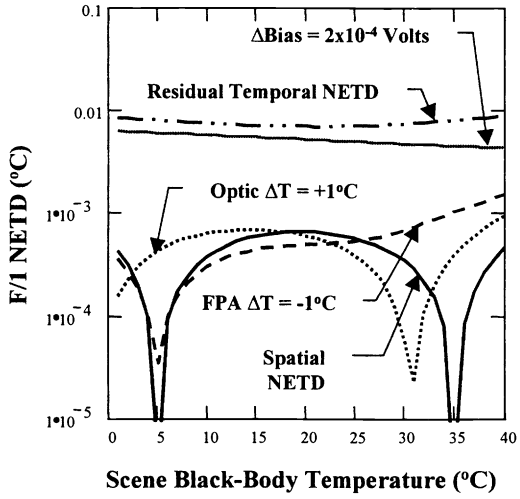

Figure2: Monte Carlo Simulation Analysis of U4000 Spatial NETD (F/1)

The effect of a shift in optics temperature can also be seen in Figure-2. Here it was assumed that the focal plane had no stray thermal radiation shield, so that the FPA was fully exposed to the optic's thermal environment. As expected, the NETD curve shifted the equivalent of 5°C to the left for a +1°C change in temperature of the F/1 optics enclosure. For bigger temperature shifts, and with slower optics, the effect on spatial NETD would be correspondingly larger. This is the reason it's often desirable to incorporate stray thermal radiation shields in the focal plane package. The analysis also indicates that the focal plane's spatial NETD performance should be relatively stable for focal plane operating temperature shifts on the order of ± 1°C. This represents a significant improvement in predicted temperature stability of the U4000 design relative to earlier uncooled focal plane designs.

U4000 PERFORMANCE MEASUREMENT AND ANALYSIS

Measurement of focal plane responsivity, noise, and both temporal and spatial NETD has been performed on the first lot of U4000 focal planes processed at Boeing. All of the measurements were performed at a nominal frame rate of 60Hz, for a focal plane operating temperature of 27°C (300K). The results are reported for an F/1 optics normalized to an optics transmission of unity. At the maximum on-chip gain setting the focal plane responsivity was 39.9 mV/°C, with an RMS response uniformity of 4.1% (σ/μ). The temporal NETD measured at 60Hz was 0.028°C (F/1). Over a scene temperature calibration range of 10°C, the spatial NETD was < 0.016°C.

The histogram of focal plane responsivity is shown in Figure-3. The average responsivity was within 15% of design prediction.. The NETD histogram for the same U4000 focal plane is shown in Figure-4, and it is essentially Gaussian with a σ/μ of 15%. Figure-5 shows a plot of the focal plane's measured RMS noise plotted as a function of the on-chip signal gain. The figure also includes the expected focal plane RMS noise based on design modeling. Here the agreement between measurement and analysis is generally excellent.

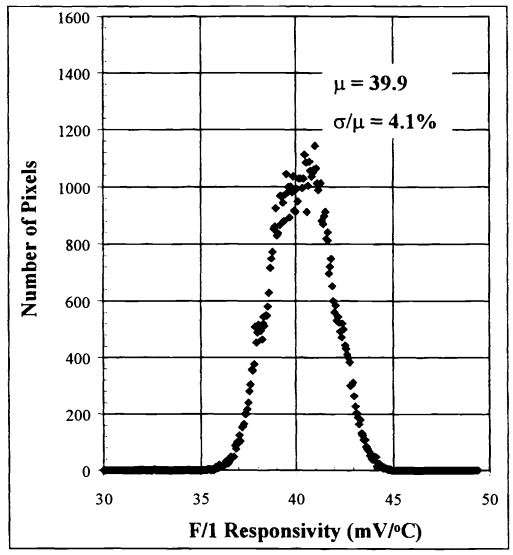

Figure 3: U4000 Responsivity Histogram

Figure-6 shows the focal plane's spatial and temporal NETDs plotted as functions of the scene blackbody temperature. The data was obtained by first performing a 2-point pixel gain and offset calibration at 10°C and 20°C, and later measuring the calibrated focal plane response as a function of temperature. The spatial NETD was determined by computing both the standard deviation and the responsivity of the pixel gain and offset compensated response for each temperature, and then calculating the spatial NETD using

$$NETD_{SPATIAL} = \sigma/\text{Responsivity}$$

Averaging 20 frame samples for each pixel was used to reduce the impact of temporal noise.

Modeling analysis predicts that the measured spatial NETD will actually be determined primarily by VO_X microbolometer 1/f noise. Although sample averaging is effective in reducing the relative contribution of broadband noise sources such as white noise, it is ineffective in reducing the relative contribution from 1/f noise. This means that the residual temporal noise should be dominated by bolometer 1/f noise after a 20-frame sample average, and that further averaging will have little effect. As a result, an irreducible error occurs in generating the initial pixel gain and offset coefficients, and a second irreducible error occurs when the normalized response is measured later. Baring other effects, such as the camera drift related effects described previously, the shape of measured spatial NETD curve should be similar to that of the temporal NETD curve.

The performance results on the first U4000 lot were significantly limited by a process control problem at the commercial CMOS process foundry that fabricated the ROIC wafers. Each of the ROIC chips exhibited exceptionally high levels of systematic threshold variation. The threshold variation measured at Boeing ranged from 50 mV to 150 mV, in contrast to an expected range of < 10 mV. Consequently, both the maximum detector bias and integration time at 60 Hz had to be limited

to about 2/3rds of their baseline design values. In fact, the level of performance demonstrated was made possible only because of the on-chip pixel offset compensation incorporated in the design of the U4000. Both the temporal and the spatial NETDs were impacted. The temporal NETD was impacted by the limitation that had to be imposed on bias and integration time, and the spatial NETD was impacted by the high level on offset non-uniformity caused by the threshold variations. The next ROIC wafer lot has been delivered from the foundry, and wafer probe testing at Boeing confirms that the threshold problem has been eliminated. Figure-7 shows the NETD performance that can be expected from the next U4000 lot. For reference, the experimental NETD measured on Lot-1, and design-modeling predictions for Lot-1 are also shown. Given the good agreement between prediction and measurement that has already been established both for responsivity and noise, a near term demonstration of NETD ~ 0.015°C (F/1) is clearly indicated.

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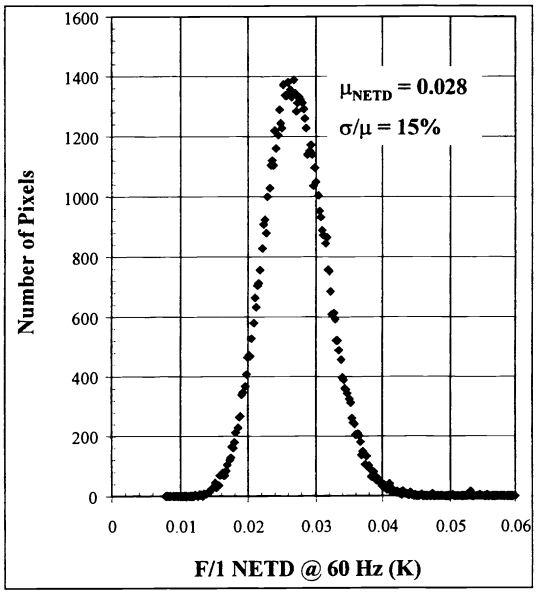

Figure 4: U4000 NETD (F/1) Histogram

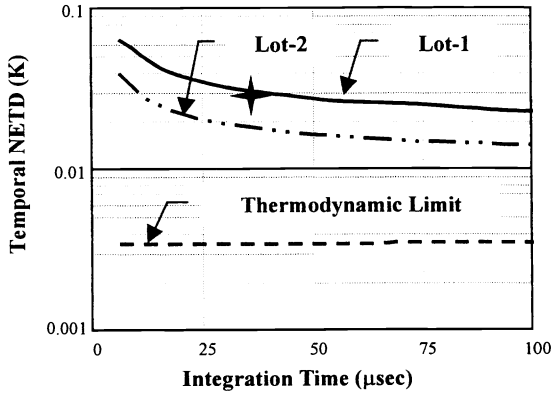

Figure 7: Measured and Projected U4000 Focal Plane NETD Performance

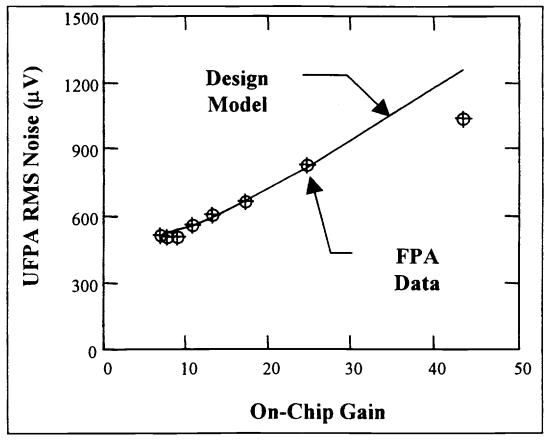

Figure 5: Focal Plane RMS Noise as a Function of On-Chip Gain (Measurement and Analysis)

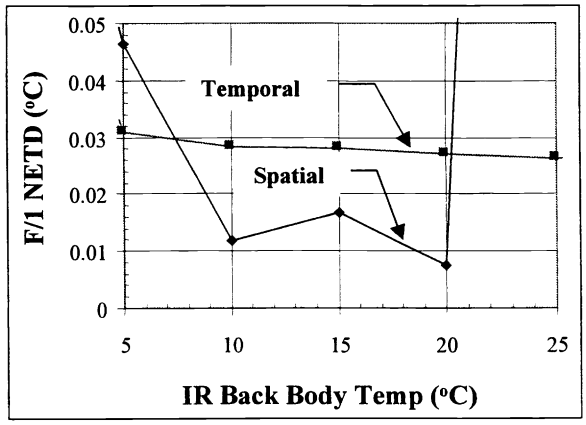

Figure 6: Measured Spatial and Temporal NETD for the Lot-1 U4000 Focal Plane